Description

BASEBAND I AND Q CONVERTER AND METHOD FOR PERFORMING BASEBAND I AND Q CONVERSION

Reference to Provisional Application

This application claims the benefit of the US Provisional Application No. 60/224,950, filed August 11, 2000.

Technical Field

The present invention relates to methods and apparatus for conversion of radio signals, and more particularly, to method and apparatus for conversion of intermediate frequencies to baseband frequencies in a radio receiver.

Background of the Invention

In the prior art it is known to convert an intermediate frequency (IF) signal to baseband signals by down-sampling the output of a band pass filter (BPF) having a delayed output and a non-delayed output. This is shown in Figure 1, which is a block diagram of a signal converter known in the prior art.

The converter 100 receives an analog signal at the input to an analog-to-digital (A/D) converter 102 which operates at a sampling frequency F_{s0}. The digital signals from the A/D converter 102 pass through a band pass frequency (BPF) 104, whose output is passed through a 1/N down sampler 106 on input 108. The output of the BPF 104 is also passed through a delay element 110, whose output is passed through the 1/N down sampler 106 on input 112. The delay created by the delay element 110 must be exactly 1/4 of the sampling time period of the carrier frequency of the signal (i.e., $1/(4f_0)$, where f_0 is the carrier frequency of the signal) to reflect the 90 degree phase shift.

The 1/N down sampler 106 has two samplers - one for each of the inputs 108 and 112. The outputs of the samplers are respectively placed on outputs 114 and 116 of the 1/N down sampler 106. The outputs are then passed through the two respective low pass filters (LPFs) 118 and 120 to generate the I and Q signals.

It is inherently difficult to generate an exact clock delay with the desired resolution in a digital system. Accordingly, it is desirable to implement a converter in a manner that does not require the production of a precise delay.

Summary of the Invention

According to one aspect, the invention is a converter for converting an intermediate frequency (IF) signal to a baseband signal, the IF signal having a center frequency of f_0 and bandwidth R. The converter includes a Σ-Δ A/D converter for converting the IF signal to an output signal by sampling the IF signal at a sampling rate F_{s0}, where $F_{s0} = f_0/N$ (N an integer) and $F_{s0} > R$. The converter also includes a first band pass filter for producing an I signal, the first band pass filter including a first finite-impulse response (FIR) filter operating at a sampling rate F_{s2}, where $R \leq F_{s2} < F_{s0}$; and a second band pass filter for producing a Q signal, the second band pass filter including a second FIR filter operating at the sampling rate F_{s2}, such that the phases of the I and Q signals differ by 90 degrees.

According to another aspect, the invention is a method for converting an intermediate frequency (IF) signal to a baseband signal, the IF signal having a center frequency of f_0 and bandwidth R. The method includes the step of a) converting the IF signal to an output signal by using a Σ-Δ A/D converter for sampling the IF signal at a sampling rate F_{s0}, where $F_{s0} = f_0/N$

(N an integer) and $F_{s0} > R$. The method also includes the step of b) producing an I signal by passing the output signal through a first band pass filter including a first finite-impulse response (FIR) filter operating at a sampling rate F_{s2}, where $R \leq F_{s2} < F_{s0}$. The method also includes the step of c) producing a Q signal by passing the output signal through a second band pass filter including a second FIR filter operating at the sampling rate F_{s2}, such that the phases of the I and Q signals differ by 90 degrees.

According to yet another aspect, the invention is a converter for converting an intermediate frequency (IF) signal to a baseband signal, the IF signal having a center frequency of f_0 and bandwidth R. The converter includes means for converting the IF signal to an output signal by using a Σ-Δ A/D converter for sampling the IF signal at a sampling rate F_{s0}, where $F_{s0} = f_0/N$ (N an integer) and $F_{s0} > R$. The converter also includes means for producing an I signal by passing the output signal through a first band pass filter including a first finite-impulse response (FIR) filter operating at a sampling rate F_{s2}, where $R \leq F_{s2} < F_{s0}$. The converter further includes means for producing a Q signal by passing the output signal through a second band pass filter including a second FIR filter operating at the sampling rate F_{s2}, such that the phases of the I and Q signals differ by 90 degrees.

Brief Description of the Drawings

Figure 1 is a block diagram of an I and Q converter known in the prior art.

Figure 2 is a block diagram of a first preferred embodiment of an improved I and Q converter in accordance with the present invention.

Figure 3 is a block diagram of a second preferred

embodiment of an improved I and Q converter in accordance with the present invention.

Detailed Description of the Preferred Embodiment of the Invention

Figure 2 is a block diagram of a first preferred embodiment of an improved I and Q converter in accordance with the present invention. This converter 250 can be used to convert from an IF to baseband I and Q signals. The converter 250 includes a sigma-delta analog-to-digital (Σ-Δ A/D) converter 202, and BPF filter blocks 220 and 240. The BPF filter blocks 220 and 240 receive their inputs from the Σ-Δ A/D converter 202, which operates at a sampling rate F_{s0}.

In operation, the converter 250 receives an incoming signal 200 having a center frequency of f_0 and bandwidth R. The incoming signal 200 is digitized by Σ-Δ A/D converter 202 at a sampling rate F_{s0}, $F_{s0} = f_0/N$ and $F_{s0} > R$. The output of Σ-Δ A/D converter 202 is band pass filtered by the BPF filter blocks 220 and 240. Each of the BPF filter blocks 220 and 240 includes a finite-impulse response (FIR) filter. BPF filter block 220 includes the FIR filter 222 (FIR-i), and BPF filter block 240 includes the FIR filter 242 (FIR-q). The BPF filter blocks 220 and 240 operate at the sampling rate F_{s2}, $R \leq F_{s2} < F_{s0}$, and respectively generate the I and Q signals 226 and 246.

The BPF filter blocks 220 and 240 have identical frequency responses, except that their time domain responses are 90 degrees out of phase. The FIR filter 222 can be designed by using a typical low pass filter (LPF) design process to obtain the impulse response of the FIR. The bandwidth of the LPF is greater than or equal to R/2. Next, the LPF impulse response is multiplied by a sine function having a center frequency of f_0.

As an example of typical LPF design, a brick wall filter can be designed using a SINC function (sin x/x), and the resulting impulse response is truncated by a conventional window function such as the Hamming window.

The FIR filter 242 can designed with the same procedure except that the LPF impulses response is multiplied by a cosine function having a center frequency of f_0.

Depending on the bandwidth of FIR filters 222 and 224, additional bandlimiting can be provided by post demodulation LPFs.

Figure 3 is a block diagram of a second preferred embodiment of an improved I and Q converter in accordance with the present invention. The converter 350 is very similar to the converter 250 shown in Figure 2. The converter 350 includes a sigma-delta analog-to-digital (Σ-Δ A/D) converter 302, and BPF filter blocks 320 and 340. The BPF filter blocks 320 and 340 receive their inputs from the Σ-Δ A/D converter 302, which operates at a sampling rate F_{s0}.

In operation, the converter 350 receives an incoming signal 200 having a center frequency of f_0 and bandwidth R. The incoming signal 200 is digitized by Σ-Δ A/D converter 302. The output of Σ-Δ A/D converter 302 is band pass filtered by the BPF filter blocks 320 and 340. Each of the BPF filter blocks 320 and 340 includes a finite-impulse response (FIR) filter and an infinite-impulse response (IIR) filter. BPF filter block 320 includes the FIR filter 322 (FIR-i) and the IIR filter 324. The BPF filter block 340 includes the FIR filter 342 (FIR-q) and the IIR filter 344.

The IIR filters 324 and 344 reduce the computational power required to implement the BPF blocks 320 and 340. The signal 304 entering the BPF block 320 is first filtered by the FIR BPF 322

for an initial bandwidth reduction. The bandwidth reduced signal is down sampled at F_{s1} samples per second and filtered by the IIR BPF 324. Further bandwidth reduction by the IIR BPF 324 allows the signal to be down sampled to produce output signal 324 at the final sampling rate F_{s2}. The BPF block 340 is implemented in a similar manner except that FIRs 322 and 342 are designed with the earlier mentioned principle to produce output with 90 degrees phase shifts.

The BPF filter blocks 320 and 340 operate at the sampling rate F_{s2} and respectively generate the I and Q signals 326 and 346.

Although the present invention is described as using a Σ-Δ A/D converter, it works well with all types of A/D converters. Advantages of using a Σ-Δ A/D converter include its over-sampling and one-bit output.

While the foregoing is a detailed description of the preferred embodiment of the invention, there are many alternative embodiments of the invention that would occur to those skilled in the art and which are within the scope of the present invention.